## REMARKS

Claims 1-20 are pending.

Claims 5-20 are withdrawn from consideration; however, claims 5-10 are species that are covered by generic claim 1.

Claims 1-4 are rejected.

Claims 1-4 are rejected under 35 U.S.C. 102(a).

Claims 2-3 are rejected under 35 U.S.C. 103(a).

Claims 1 and 5 have been amended.

No new matter is added.

Claims 1-10 remain in the case for consideration.

Applicant requests reconsideration and allowance of the claims in light of the above amendments and following remarks.

**Election/Restrictions**

Applicant's election with traverse of Species 1A, claims 1-4, in the reply filed on January 26, 2006 is acknowledged. The Applicants note that although claims 5-10 are not currently being examined pursuant to the claim restriction, they are included (and claim 5 is amended) in this Response so that amended claim 1 remains generic in view of claims 5-10.

**Examiner Interview**

An Examiner Interview was conducted May 11, 2006 between Mr. Gregg Palmer as a representative for the Applicants and Examiner Douglas Menz. During the interview Mr. Palmer and Examiner Menz discussed the relationship between claim 1 and the Applicants' Admitted Prior Art, and in particular the differences shown between FIGs. 5B and 9B. Examiner Menz indicated that the protective layer (element 224 of FIG. 9B) did not appear to be taught by the prior art, but suggested that claim 1 be amended to more clearly distinguish this element.

**In the Specification**

The specification has been amended to correct informalities and improve consistency with the written specification. No new matter has been added. In particular, the following has

been amended in the specification: 1) Page 8, line 10 has been amended to correct the final paragraph of the "Brief Description of Drawings" to read "FIGS. 6A through 9D" instead of "FIGS. 6A through 6D" to be consistent with the actual number of drawings and their related description. 2) Page 10, line 31 has been amended to add the element label "234" after "third interlevel dielectric layer" for clarity purposes. 3) Page 10, line 32 has been amended to delete the first instance of the label "234" located in the phrase "that of 234 the bit line" for clarity purposes.

**In the Drawings**

Figures 8D and 9D have been amended to replace the element labels "222" with "224" and to correctly shade the layer that the above element labels refer to. In particular, these layers are the same protective layer "224" shown in FIG. 7. However, because of an error in drafting, the protective layer 224 was not properly represented in FIGs. 8D and 9D. This correction is further supported in the specification. For example, page 11, lines 28-29 state that "during the etching, regions around the second contact pads 216 can be protected by the protective layer pattern 224." This example statement from the specification shows that the protective layer 224 is not removed and replaced by the second interlevel dielectric layer as would otherwise be suggested by the illustrated differences between Figures 7D and 8D.

**In the Claims**

**Claim Rejections – 35 U.S.C. § 102**

Claim 1-4 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's Admitted Prior Art (APA). Claim 1 has been amended and is set out below in amended form. In claim 1, a semiconductor memory device with a capacitor on a bit line (COB) cell structure comprises:

a semiconductor substrate including an isolation region that defines an active area with a plurality of source/drain regions;

a contact pad layer formed on the semiconductor substrate, said contact pad layer including gate line structures, first contact pads connected to parts of the source/drain regions, second contact pads connected to the other source/drain regions, and a first interlevel dielectric layer formed to cover the gate line structures and formed to laterally surround the first and second contact pads;

a bit line contact plug layer on the contact pad layer, said bit line contact plug layer including lower storage node contact plugs connected to the first contact pads, bit line

contact plugs connected to the second contact pads, a protective layer pattern that covers at least a portion of the second contact pads to prevent the second contact pads from contacting the lower storage node contact plugs, and a second interlevel dielectric layer formed to laterally surround the lower storage node contact plugs, the bit line contact plugs, and the protective layer pattern; and

a bit line layer formed on the bit line contact plug layer, said bit line layer including upper storage node contact plugs connected to the lower storage node contact plugs, bit line structures connected to the bit line contact plugs, and a third interlevel dielectric layer formed to laterally surround the upper storage node contact plugs and formed to laterally surround and cover the bit line structures.

In particular, claim 1 includes the limitation of a protective layer pattern that covers at least a portion of the second contact pads to prevent the second contact pads from contacting the lower storage node contact plugs, and a second interlevel dielectric layer formed to laterally surround the lower storage node contact plugs, the bit line contact plugs, and the protective layer pattern.

In contrast, the APA does not teach or otherwise disclose this protective layer. In the Office Action, the Examiner states that the protective layer pattern is taught by element 122 of FIG. 4D. However, the Applicants respectfully point out that this layer merely teaches a second interlevel dielectric layer, which the background clearly states. In addition, claim 1 has been amended to further clarify this distinction between the protective layer pattern and the second interlevel dielectric layer. Referring to FIG. 4B of the APA, the Applicants point out that the APA fails to teach a protective layer pattern that covers at least a portion of the second contact pads and a second interlevel dielectric layer formed to laterally surround the lower storage node contact plugs, the bit line contact plugs, and the protective layer pattern. Thus, because the APA does not teach all of the limitations of claim 1, it cannot anticipate claim 1. As such, the Applicants submit that claim 1 is in allowable form and request that the rejection under § 102(a) be removed.

Claims 2-4 depend from claim 1. Based at least on this dependency, the Applicants submit that claims 2-4 are likewise in proper form for allowance.

Claim 5 has not been examined; however, the Applicants have amended claim 5 so as to insure that amended claim 1 remains generic in view of claim 5.

**Claim Rejections – 35 U.S.C. § 103**

Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (APA).

As mentioned above with respect to the § 102(a) rejection, the APA does not teach at least the protective layer claimed in claim 1. Thus, based at least on their dependency to claim 1, the Applicants submit that claims 2-3 are likewise in proper form for allowance.

**Conclusion**

For the foregoing reasons, reconsideration and allowance of claims 1-10 of the application as amended is requested. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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